

EE 232.3 Digital Electronics

Instructor: **Dr. Khan Wahid**
 Office: 2B46, Engineering Building
 Office Hours: Wednesday (1.00pm – 2.30pm)
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Class Location: 1B79, Engineering Building, Class Schedule: Lecture – M W F (9.30am – 10:20am)

- **Official Course Description:**

(3L) An introduction to digital logic including combinational and sequential logic devices and circuits. It covers the range from the fundamentals of Boolean algebra and the binary number systems to combinational and sequential circuit functional blocks such as adders, multiplexers, counters, and state machines. Some coverage is also given to electronic characteristics of real logic devices and field programmable gate arrays (FPGA).

Prerequisite(s): EE 221

- **Purpose of the Course:**

The main purpose of the course is to study the principles and applications of modern Digital Electronics. The course will cover the fundamentals of digital system design (i.e. combinational and sequential circuit elements) using both traditional and modern design techniques. Introductory concepts of Hardware Description Language (HDL) will be taught and small digital circuits will be built using Verilog HDL.

- **Text Books:**

- **Digital Systems: Principles and Applications, Tocci, Widmer and Moss, 10E, ISBN: 0131725793**
- Supplements: (Additional materials and excerpts from these books will be handed out in the class)
 - Fundamentals of Digital Logic with Verilog Design, Brown and Vranesic, 2E, ISBN: 9780073380339
 - Digital Design, Mano and Ciletti, 4E, ISBN: 0131989243
 - Digital Design, Frank Vahid, 1E, 2006

- **Course Evaluation:**

The course evaluation is as follows:

○ Assignments (8):	16%
○ Quizzes (3):	15%
○ Lab Assignments (2):	4%
○ Midterm (1):	25%
○ Final Exam (1):	40%

Total:	100%
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- **Missed Exam Policy:**

There will be assignments (shorts questions, problems, MCQ, etc.) every week and quizzes on every 3rd week. If a student misses an exam or assignment deadline, a ZERO score will be assigned. All weekly assignments are due on Friday (following week) by noon. Assignments should be dropped in appropriate box (located in front of 2C94). There will be two lab assignments; part of these lab assignments will be completed during lab sessions (which will be arranged in place of regular class hours). The student must attend the lab sessions in order to get any credit for lab assignments.

- **Plagiarism and Academic Dishonesty:**

Plagiarism is defined as per the UofS calendar: *“the presentation of the work or idea of another in such a way as to give others the impression that it is the work or idea of the presenter. Examples of plagiarism are: (i) The use of material received or purchased from another person or prepared by any person other than the individual claiming to be the author. [It is not plagiarism to use work developed in the context of a group exercise (and described as such in the text) if the mode and extent of the use does not deviate from that which is specifically authorized]. (ii) The verbatim use of oral or written material without adequate attribution; (iii) The paraphrasing of oral or written material of other persons without adequate attribution.”*

If the student is judged guilty of the offense, a penalty will be applied. For help with interpreting plagiarism and other academic dishonesty rules, see the Academic Honesty website: www.usask.ca/university_secretary/honesty/index.php

More on plagiarism can be found here:

www.usask.ca/university_secretary/pdf/dishonesty_info_sheet.pdf

www.winthrop.edu/wcenter/handoutsandlinks/plagiar.htm

www.hamilton.edu/writing/sources.html

www.commerce.usask.ca/classes/2006Term2/comm100/academichonesty.html

- **Tentative Course Schedule:** (The schedule and syllabus are subject to change any time at Instructor's discretion)

Week (Days)	Lecture Topic	Chapter	Assignment / Quiz / Exam
Week 1 (3) Jan 5, 7, 9	Introductory concepts, Digital number systems, number codes, Boolean algebra, logic gates, Boolean theorems	Chapter 1, 2, 3	Assignment 1
Week 2 (3) Jan 12, 14, 16	Gate level minimization, K-map, Combinational logic circuits, problem solving	Chapter 4	Quiz 1
Week 3 (3) Jan 19, 21, 23	Digital arithmetic: 2's complement, half-adder, full-adder, Subtractor, BCD adder, multiplier	Chapter 6 Mano (Ch 4) Vahid (Ch 6)	Assignment 2
Week 4 (3) Jan 26, 28, 30	MSI logic circuits: decoder, encoder, multiplexer, comparator	Chapter 9 Mano (Ch 4)	Assignment 3 Quiz 2
Week 5 (3) Feb 2, 4, 6	Synchronous sequential logic: Flip-Flops and related devices	Chapter 5 Vranesic (Ch 7) Vahid (Ch 3)	Assignment 4
Week 6 (3) Feb 9, 11, 13	FF timing considerations, propagation delay, critical path, Midterm Review	Chapter 5	Midterm Exam (TBA) Assignment 5
Week 7 (0) Feb 16-20	No Class	Midterm Break	No Class
Week 8 (3) Feb 23, 25, 27	Introduction to HDL and CAD tools, circuit design with Verilog HDL	--	Assignment 6
Week 9 (3) Mar 2, 4, 6	Registers, counters	Chapter 7	Assignment 7 Lab Assignment 1
Week 10 (3) Mar 9, 11, 13	Circuit design with HDL, Sequential circuit analysis with state diagrams, Finite State Machine, Hazards in digital circuits	Chapter 7 Vranesic (Ch 8)	Assignment 8 Quiz 3
Week 11 (3) Mar 16, 18, 20	IC logic family, TTL characteristics, Inverter operation	Chapter 8	Lab Assignment 2
Week 12 (3) Mar 23, 25, 27	Memory devices, DRAM, SRAM, ROM, Circuit design with HDL	Chapter 12 Mano (Ch 7) Vahid (Ch 5)	
Week 13 (3) Mar 30, Apr 1, 3	Memory devices, Programmable logic devices, PLA, FPGA	Chapter 12, 13 Vranesic (Ch 3)	--
Week 14 (2) Apr 6, 8	FPGA, Review of all materials, Exam Review	--	--
TBA	Final Exam	--	TBA

Last updated on February 19, 2009