CHAPTER 1: OP-AMPS

I. PRACTICAL OP-AMP

An operational amplifier, or op-amp, is an electronic device having very high gain differential amplifier, $A$, high input impedance, $Z_{\text{in}}$, and low output impedance, $Z_{\text{out}}$ as shown in Figure a. Typical uses of op-amp are to provide voltage amplitude changes (amplitude and polarity), oscillators, filter circuits, and many types of instrumentation circuits. Figure below shows a schematic diagram and a symbol of an op-amp.

![Op-amp schematic diagram](image1)

**Figure a:** Op-amp schematic diagram

![Op-amp symbol](image2)

**Figure b:** Symbol of an op-amp

The op-amp operates using two power supplies, $+V_{\text{CC}}$ and $-V_{\text{EE}}$, (some op-amps can operate using a single supply, i.e., $-V_{\text{EE}}$ is grounded). The op-amp input, $v_{\text{in}}$, to the differential amplifier is the difference between two input voltages: the *non-inverting* input and the *inverting* input.
input. The op-amp has a *single-ended output*. Op-amp also has an input impedance, $z_{in}$, an output impedance, $z_{out}$, and a *voltage gain* $A$ as shown in the schematic diagram above.

The output voltage of the op-amp can be express in term of the input voltage and the gain of the amplifier as:

$$v_o = Av_{in}$$

A typical op-amp has very high gain, very high input impedance ($z_{in}$ is in the range of $M\Omega$) and very low output impedance ($z_{out}$ is less than $100\Omega$).

Below is a simple block diagram of an op-amp. The *differential amplifier* takes two inputs and amplifies the difference, the *gain stage* contains many amplification stages to achieve high gain of the op-amp and the *output stage* (a class B amplifier) provides high current gain with low output impedance.

1. **Input characteristics of an op-amp**

   1. Input bias current

      Since the $\beta_{DC}$ of each transistor in the first stage is slightly different, the base currents in the differential amplifier above are slightly different. The input bias current is defined as the average of the DC base currents:

      $$I_{in(base)} = \frac{I_{B1} + I_{B2}}{2}$$

      The bias current is typical in nano-amperes (BJT) or pico-amperes (FET) and will flows through the resistances between the bases and ground. These resistances may be discrete resistances or they may be the Thevenin resistances of the input sources.
2. **Input offset current**

The input offset current is defined as the difference of the DC base currents:

\[ I_{\text{in}(\text{off})} = I_{B1} - I_{B2} \]

This difference in the base currents indicates how closely the transistors Q1 and Q2 are matched. If the transistors are identical, the input offset current is zero because both base currents will be equal, but almost always, the two transistors are slightly different and the two base currents are not equal.

Data sheet of an op-amp lists \( I_{\text{in}(\text{base})} \) and \( I_{\text{in}(\text{off})} \), the base current through each transistor can be calculated using two equations above. The base currents can cause output voltage error in precision applications. A compensate resistor may be used to eliminate the effect of the input offset current as shown in Figure 17-14b.

![Figure 17-14](image)

**Figure 17-14:** a) Base resistor produces unwanted input voltage; b) equal base on other side reduces error voltage

3. **Input offset voltage**

More errors caused by the imperfect match of the differential amplifier stage are collector resistances \((R_{C1} \neq R_{C2})\) and base-emitter voltages \((V_{BE1} \neq V_{BE2})\) as shown in figure below.

![Figure](image)
The input offset voltage is defined as the input voltage that would produce the same output error voltage in a perfect differential amplifier.

\[
V_{\text{in (off)}} = \frac{V_{\text{error}}}{A}
\]

**Figure 17-16:** Output of diff amp includes desired signal and error voltage

Total error:

\[
V_{\text{in}} = v_1 - v_2
\]

\[
V_{\text{out}} = A(v_1 - v_2)
\]

DC error inputs:

\[
V_{1\text{err}} = (R_{B1} - R_{B2})I_{\text{in (bias)}}
\]

\[
V_{2\text{err}} = (R_{B1} + R_{B2})I_{\text{in (off)}}/2
\]

\[
V_{3\text{err}} = V_{\text{in (off)}}
\]

\[
V_{\text{err}} = A(V_{1\text{err}} + V_{2\text{err}} + V_{3\text{err}})
\]

**Table 3:** Sources of Output Error Voltage

<table>
<thead>
<tr>
<th>Description</th>
<th>Cause</th>
<th>Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input bias current</td>
<td>Voltage across a single (R_B)</td>
<td>Use equal (R_B) on other side</td>
</tr>
<tr>
<td>Input offset current</td>
<td>Unequal current gains</td>
<td>Data sheet nulling methods</td>
</tr>
<tr>
<td>Input offset voltage</td>
<td>Unequal (R_C) and (V_{BE})</td>
<td>Data sheet nulling methods</td>
</tr>
</tbody>
</table>
2. **The 741 op-amp**

Some noticeable characteristics on this industry standard op-amp are useful to design op-amp application circuits:

*a. The final stage*

The quiescent output is ideally 0V when the input voltage is zero (assuming an equal positive and negative supply voltages). Any deviation from 0V is called the output error voltage.

The output swing is within 1 to 2V of each supply voltage because of voltage drops inside the op-amp.

*b. Frequency compensation*

The capacitor $C_C$ is a compensating capacitor. Miller effect causes this capacitor become a large input capacitance of:

$$C_{in} = (A+1)C_C$$

where $A$ is the gain of Q5 and Q6.

This capacitor generates a cutoff frequency of 10Hz and the op-amp has an ideal Bode plot as shown in the figure below.
c. *Bias and offsets*

Figure below shows the compensation and nulling used with 741C op-amp. The resistor $R_B$ neutralizes the effect of input bias current (80nA). The 10K potentiometer is used to null or zero the output voltage with no input signal present. This eliminates the effect of an input offset current of 20nA and an input offset voltage of 2mV.

![Bias and offsets circuit](image)

\[ +V_{CC} \]
\[ 741C \]
\[ V_{out} \]
\[ -V_{EE} \]
\[ R_B \]
\[ R_B \]
\[ 10 \text{ k}\Omega \]

---

d. **CMRR (Common Mode Rejection Ratio)**

The CMMR is 90dB at low frequency but degrades at higher frequency according to the curve (a) below.

![CMRR graph](image)

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e. **Maximum peak-to-peak output**

The maximum peak-to-peak output voltage produced by 741 op-amp depends on the load resistance connected to its output as shown in curve (b).

![Maximum peak-to-peak output graph](image)

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f. **Short circuit current**

The maximum short circuit current at the output which the 741 op-amp can withstand is 25mA. This is also the maximum current can be produced by the op-amp and delivered to the load.
g. **Frequency response**

Curve (c) shows the actual frequency response of the 741 op-amp with a unity frequency of 1MHz. This op-amp is considered worthless for higher frequency applications (i.e., attenuation instead of gain). Other op-amps are available for use at high frequency.

h. **Slew rate**

The compensation capacitor, $C_C$, prevents oscillations (capacitor $C_C$ acts as negative feedback) that would interfere with the desired signal. However, this capacitor also creates a speed limit on how fast the output of the op-amp can change. This relates to the slew rate of the op-amp which is defined as:

$$S_R = \frac{\Delta V_{out}}{\Delta t}$$

where $S_R$ is the slew rate and equals to the change in output voltage divided by the change in time.

The slew rate represents the fastest response that an op-amp can have. The 741C has a slew rate of 0.5V/μs. This means that the output of a 741C can change no faster than 0.5V in a microsecond (figure (c) above). Slew rate also affects the response of sinusoidal signal as shown in the figure below.

Slew rate limits large-signal response of an op-amp and this quantity always specifies in the data sheet. The initial slope of a large sinusoidal signal, can be derived as:
To avoid slew-rate distortion, $S_S$ has to be less than or equal to $S_R$ of the op-amp. The maximum frequency at which the signal is on the verge of slew-rate distortion can be found as:

$$S_R = S_S = 2\pi f_V$$

$$f_{max} = \frac{S_R}{2\pi V_p}$$

This frequency is sometimes called the *power bandwidth or large-signal bandwidth* of the op-amp. Therefore, there are two bandwidth to be considered when analyzing the operation of an op-amp circuit: the small-signal bandwidth determined by the first order response of the op-amp (by compensation capacitor $C_C$) and the large-signal or power bandwidth determined by the slew rate $S_R$.

*Example : 18-1 to 18-4 (page 628).*

II. **IDEAL OP-AMP**

To analyze circuits using op-amps, the ideal op-amps are used to simplify the process. Some characteristics of the ideal op-amp are:

- Gain $A = \infty$
- $Z_{in} = \infty$
- $Z_{out} = 0$
- Input currents $I_+ = 0$
- Input current $I_- = 0$
- $v_a = v_+ - v_- = 0$

because $v_a = A v_a$,
$v_a = v_o/A = v_o/\infty$

i.e., *operation depends on external connection.*
1. INVERTING AMPLIFIER:

The inverting amplifier is an important op-amp circuit. The inverting amplifier uses negative feedback to stabilize the overall voltage gain of the amplifier because the open-loop gain of the op-amp is too high and the circuit will be unstable to be used without some forms of feedback. The circuit is analyzed as below using the ideal op-amp characteristics.

Because of $I_+=I_-=0$, $v_a=0$:

\[ v_a = 0 \Rightarrow i_{in} = \frac{v_{in}}{R_2} \]
\[ I_+ = I_- = 0 \Rightarrow i_{R1} = i_{in} = \frac{v_{in}}{R_2} \]
\[ v_o = -i_{R1}R_1 = -v_{in} \frac{R_1}{R_2} \]
\[ v_o = -v_{in} \frac{R_1}{R_2} \]

Gain : $A_{(CL)} = -\frac{R_1}{R_2}$
\[ z_{in(CL)} = R_2 \]
\[ f_2(CL) = \frac{f_{unity}}{A_{CL}} \]

The plot of the inverting amplifier gain versus frequency is shown below. The op-amp has an open loop gain, $A_{(OL)}$, and an open loop cutoff frequency $f_{2(OL)}$. For the feedback configuration, the amplifier has a close loop gain, $A_{(CL)}$, and a close loop frequency $f_{2(CL)}$. When the gain is 0dB (i.e., gain=1=unity), the amplifier has a frequency of $f_{unity}$.

Example: 18-7
2. NON-INVERTING AMPLIFIER:

This feedback amplifier provides an output voltage in phase with the input voltage. The analysis of this circuit also uses the ideal op-amp.

\[
\begin{align*}
    i_{R2} &= \frac{v_{in}}{R2} \\
    I_- &= 0 \Rightarrow i_{R1} = i_{R2} \\
    v_o &= v_{in} + i_{R2}R1 = v_{in} + \frac{v_{in}}{R2}R1 \\
    v_o &= v_{in}(1+\frac{R1}{R2}) \\
    \therefore \text{Gain:} \quad A_{CL} &= 1 + \frac{R2}{R1}
\end{align*}
\]

*Example: 18.10*

3. SUMMING AMPLIFIER:

\[
v_o = -(\frac{R3}{R1}v_1 + \frac{R3}{R2}v_2)
\]

*Example: 18-12*

*Problem: 18-22, 18-26*

*Try: 18-9, 18-11, 18-13, 18-21, 18-23, 18-27*
4. **INTEGRATOR**

The output of the integrator is proportional to the integral over time of its input signal (example, a constant input $v_i$ yields a ramp output).

\[ v_o = -\frac{1}{RC} \int v_i dt \]

5. **DIFFERENTIATOR**

The output of the integrator is proportional to the differential over time of its input signal (example, a ramp input $v_i$ yields a constant output).

\[ v_o = -RC \frac{dv_i}{dt} \]

6. **INSTRUMENTATION AMPLIFIER**

\[ A = \frac{(2R_b + R_a)R_d}{R_a R_c} \]