Part I – PCM & Quantization Noise

Safety: In this lab, voltages are less than 15 volts and this is not normally dangerous to humans. However, you should assemble or modify a circuit when power is disconnected and don’t touch a live circuit if you have a cut or break in the skin.

Note: - Take time to ask questions and understand. We expect “real-time notekeeping” with very little “fix-up” after the experiment. Do not leave the lab early with an incomplete logbook.

Objective: To investigate pulse code modulation (PCM) and to observe output quality as a function of bits per sample. To investigate the benefit of oversampling.

Equipment: You will require a PCM module, a 3 kHz filter module EE32.xx (available from the technicians in 2C78 or 2C94), a spectrum analyzer (an HP 3580A, an SR770, or a ‘scope that can calculate DFT), two signal generators, a ±15 V power supply and an oscilloscope.

Prior to the laboratory review lecture material on PCM. See also virtual laboratories at the website: http://www engr.usask.ca/classes/EE/352/expindex2/VirtualLab-2f/pcm/dac.htm.

Procedure:
1. Setup - Obtain the PCM test module shown in Figure 3 and provide a 100 kHz TTL sampling clock to operate the converter. Apply a 1 kHz sinewave message signal and adjust the amplitude to match the maximum input range of the A/D converter (about 6Vpp).

   Note: If the input range of the A/D converter is exceeded, your signal will be clipped, but if it is much less than the input range then the effective number of bits will be reduced.

   Note: The clock input on this module is NOT PROTECTED. The input voltage must remain within TTL (transistor-transistor logic) levels of 0V and +4V. Do not connect a signal generator without first setting the voltage levels using an oscilloscope. Hint: the “sync” output of most generators provides a square wave with TTL levels.

2. Waveforms - With the setup of Figure 1, use the oscilloscope to observe and record the quantized signal and the error signal waveforms. Observe for different numbers of bits in the quantizer. Bit switches are described in the Appendix. LPF and distortion analyzer are not needed for this part.

Fig. 1 Block diagram of experimental set-up.

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3. **SNR vs Bits** - Set the sampling frequency at 20 kHz and, using the distortion analyzer, measure the signal-to-noise ratio (SNR) in the sampled signal after the 3 kHz low-pass filter for different $n$ bits of quantization (the expected change is 6 dB per bit).

   **Note:** To minimize discrete frequencies in the quantizing noise, avoid an integer multiple between the message signal frequency and the sampling frequency. For example, use 20.07 kHz sampling frequency. Still, substantial quantizing noise sometimes falls within, and sometimes falls outside, the 3 kHz filter. This problem might be mitigated by using a compound message signal but then SNR cannot be measured with a single distortion analyzer. Thus, with this set-up, measured SNR will deviate somewhat from 6 dB per bit.

4. **Signal Level** – With 5 quantizing bits, show that quantizing noise remains constant as signal level is reduced from full load (0 dB) to -6 dB, -12 dB and -18 dB. Observe the error signal on the `scope - does the Vp-p remain constant? Also observe noise on the spectrum analyzer. There is no need to adjust “set level” since you know the changes in the input signal level.

   Note: noise in the 3 kHz bandwidth will vary somewhat as the signal level changes or the sampling rate changes. This deviation from theory is due to the simple (predictable) sinewave input signal.

   The curve shown in Figure 2 has a 1:1 slope at signal levels less than 0 dB. This is based on the assumption that noise remains constant. As signal decreases by 10 dB, the SNR decreases by 10 dB.

5. **Oversampling** - Increasing the sampling rate improves the SNR of a band-limited PCM system (i.e. a system with a low-pass filter on the output). Verify experimentally with sampling rates 10 kHz, 20 kHz, 40 kHz and 80 kHz.

   **Questions:** Does the output DAC produce natural or flat-top samples?
   What is the duty cycle?
Appendix A - PCM Board (EE18.xx)

The circuit uses a AD7575 8-bit A/D converter to digitize the input signal. Capacitive coupling and a resistor network are used to attenuate and shift the input voltage so that the voltage applied to the A/D converter is positive.

The module also includes two 8-bit DACs and switches that allow the bits to go to either the first or the second DAC. If \( n \) higher order bits are sent to the first DAC then its output will be the \( n \)-bit PCM signal. The second DAC receives the \( 8-n \) lower order bits, and its output approximates the error signal.

Switches to the left connect to the upper DAC, switches to the right connect to the lower DAC.

Fig. 3 Schematic of the PCM module