Safety

You should always follow safe procedures when working on any electronic circuit. Assemble or modify a circuit with the power off or disconnected. Don’t touch different nodes of a live circuit simultaneously, and don’t touch the circuit if any part of you is grounded. Don’t touch a circuit if you have a cut or sore that might come in contact with a live wire. Check the orientation of polarized capacitors before powering a circuit, and remember that capacitors can store charge after the power is turned off. Never remove a wire from an inductor while current is flowing through it. Components can become hot if a fault develops or even during normal operation so use appropriate caution when touching components.

This laboratory exercise presents the following specific hazards:

Shock: Inductors and transformers can produce very high potentials when the current through them is abruptly changed (usually by opening the circuit); allow for appropriate discharge paths and insulate yourself appropriately when contacting leads or components. A node connected to an inductor should be treated as possibly at a high voltage.

Burn: Circuit elements under load, especially abnormal load caused by circuit or design errors, can reach temperatures which will cause burns to skin if contacted. Do not attempt to determine the temperature of elements with your fingers! Approach potentially overheated elements with caution and allow sufficient time for cooling when necessary. In some cases, elements may burst into flames. This is usually very isolated and does not normally create a fire hazard. If overheating does occur, immediately remove power and determine and correct the cause before re-energizing!

Explosion: Capacitors that are subjected to potentials exceeding their rating can burst their cases. Polarized electrolytic capacitors commonly used as power supply filter elements can explode if they are connected with the polarity reversed, even below the rated voltage. Make certain that all electrolytic capacitors are connected with the proper polarity before energizing the circuit.

This laboratory exercise and its manual were originally designed and written by Prof. D. Lynch with contributions and revisions from M. Nesdoly, J. Kowalski, B. Fogal, A. El Damaty, Prof. S.B. Ko, and H. Majid. The manual was revised for EE321 by Prof. R. Johanson with input from P. Pourhaj and C. Janzen.
Objectives: These experiments will investigate the operating principles and design of a switch-mode power supply (SMPS). At the end of the laboratory, a student should be able to

- explain the operation of a flyback circuit,
- semi-quantitatively explain how the output voltage depends on switching frequency and duty cycle,
- explain the importance of incorporating a transformer in the design, and
- design a simple switch-mode power supply that includes regulation.

Note: This design laboratory on switch-mode power supplies is independent of the lecture part of EE321 and is mostly self-contained. You are expected to read through the background material and understand the basic operation of a switch-mode power supply. You will then use the information to investigate the operation of sections of a SMPS and design a supply to certain specifications. The laboratory is in three parts; each part should be completed in a three hour laboratory period. The design part of the lab, part 3, requires that preparatory work be done before coming to the lab.

1 The flyback circuit

Introduction: The purpose of any d.c. voltage supply is to transform an unregulated, possibly varying voltage into a specified, stable voltage that is independent of the current drawn by the load (within limits, of course). There are various types of power supplies with the most common ones being the linear supply and the switch-mode power supply (SMPS). SMPSs have become the architecture of choice for power conversion because of their economy, high efficiency, and light weight. We begin this laboratory by investigating a core circuit in one type of SMPS without the complication of feedback regulation.

The basic operating principles of a SMPS can be illustrated by the circuit in Fig. 1, which is called a flyback or inverting configuration. Let us analyze this circuit assuming all the components are ideal.

The switch is repeatedly closed and opened at a frequency f with duty cycle η. During the first part of the cycle, the switch is closed, and the input voltage V_{in} is applied to the inductor. Recall that the fundamental equation for an inductor is V = L \, dI/dt. For a constant voltage applied to the inductor, the solution of this equation is a linear increase of the current with time, \( I = I_0 + (V_{in}/L)t \). Notice that the diode is reverse biased because of the polarity of the output voltage V_{out}. Meanwhile, on the other side of the circuit the capacitor supplies a current to the load resistor R_L. This current will partially discharge the capacitor resulting in a decrease of V_{out}. The reverse-biased diode keeps the two parts of the circuit separate.

When the switch opens, the inductor will attempt to keep the current flowing by very rapidly decreasing the voltage at node X. The voltage will continue to decrease until it reaches \(-V_{out}\) at which point the diode becomes forward biased. Current then flows through the diode and charges the capacitor resulting in an increase in V_{out}. The cycle then repeats. The current through the inductor and the voltage across the inductor are plotted in Fig. 2.
Another way to analyze the circuit is to consider the flow of energy. With the switch closed and the current increasing, energy is being stored in the magnetic field of the inductor; recall that \( W = LI^2/2 \). When the switch opens, the energy is transferred through the diode to the capacitor where it is stored in the capacitor’s electric field, \( W = CV_{\text{out}}^2/2 \). The load dissipates the energy on the capacitor at a rate given by \( P = V_{\text{out}}^2/R_L \). Notice that the load is the only place power is consumed in this ideal circuit; the capacitor and inductor store energy but do not consume any. The circuit is therefore 100% efficient. In a real circuit there are losses due to series resistances in the inductor and the switch (which is usually a MOSFET) as well as core losses in the inductor. The diode also consumes power since there is a finite voltage drop when it is conducting current in forward bias. Nevertheless, this energy transfer scheme between the inductor and the capacitor is what makes the SMPS much more efficient than a linear supply.

We now need to calculate \( V_{\text{out}} \) which we can do by equating the power transferred from the inductor to the average power dissipated by the load. The amount of energy transferred per cycle depends on the peak current in the inductor at the end of the first part of the cycle. The switch opens at time \( t = \eta/f \) and so \( I_{\text{peak}} = (V_{\text{in}}/L)(\eta/f) \) (here we assume \( I_0 = 0 \)). The peak energy in the inductor is \( W_{\text{peak}} = L(V_{\text{in}}/L)^2(\eta/f)^2/2 \). We assume that all of this energy is transferred to the capacitor during the second part of the cycle. Dividing \( W_{\text{peak}} \) by the cycle period \( 1/f \) gives the average power transferred from the inductor, \( P = (\eta V_{\text{in}})^2/(2Lf) \). In equilibrium, this power must be consumed by the load, \( P = V_{\text{out}}^2/R_L \). Equating and solving for \( V_{\text{out}} \) gives

\[
V_{\text{out}} = \eta \frac{R_L}{2Lf} V_{\text{in}}
\]
Notice how the output voltage depends on the switching frequency and the duty cycle. Since these can be easily varied, they provide a means to set and regulate the output voltage. This calculation ignores the other power losses in a real circuit, but the formula is a useful simple approximation for working with the circuit.

The above calculation assumes that all the energy on the inductor is transferred each cycle, but is this true? Full transfer of energy will occur if the current through the inductor drops to zero before the end of the cycle. The time it takes for the current to drop from $I_{\text{peak}}$ to zero is given by the equation $0 = I_{\text{peak}} - (V_{\text{out}}/L)t$ or $t = I_{\text{peak}}L/V_{\text{out}} = (V_{\text{in}}/V_{\text{out}})(\eta/f)$. This time must be less than the amount of time the switch is open $(1-\eta)/f$. This condition imposes a requirement on the duty cycle,

$$\eta < \frac{V_{\text{out}}}{V_{\text{out}} + V_{\text{in}}}$$

The calculation also assumes the output voltage is constant. Of course, if the power supply is designed properly, the output voltage should be nearly constant. However since the capacitor alternately receives and delivers charge, $V_{\text{out}}$ must vary to some extent. The amount of the variation is called the ripple. We can estimate the magnitude of the ripple by calculating the discharge from the capacitor while the switch is closed. Since the diode is reverse biased, the capacitor is simply being discharged by the load resistance, and so the output voltage will decay as an exponential function with a time constant $t = R_L C$. Since the ripple is expected to be small, we can linearize the exponential, $V_{\text{out}} = V_{\text{max}}\exp(-t/t) \sim V_{\text{max}}(1-t/t)$. So at the end of the period with the switch closed, $t = \eta/f$, the voltage will have decreased by $V_{\text{out}}(\eta/fR_L C)$ which is the ripple

$$\Delta V_{\text{out}} = \frac{V_{\text{out}} \cdot \eta}{fR_L C}$$

1.1 Some Practical Restrictions

For proper operation of a switched-mode power supply, the inductor’s current must

- stay below saturation during switch ON time. The maximum ON time is
  $$T_{\text{on max}} = \frac{L \cdot I_{\text{sat}}}{V_{\text{in}}}$$

- drop to zero during switch OFF time. The maximum duty cycle to meet this requirement is
  $$\eta_{\text{max}} = \frac{V_o}{V_o + V_{\text{in}}}$$

$I_{\text{sat}}$: Inductor’s saturation current

$V_{\text{in}}$: Input DC voltage

$V_o$: output voltage

The power is delivered to the inductor from DC input is

$$P_{\text{in}} = \frac{V_{\text{in}} \cdot I_{\text{peak}} \cdot T_{\text{on}} \cdot f}{2} = \frac{V_{\text{in}}^2 \cdot T_{\text{on}} \cdot \eta}{2L}$$

By rearranging the equation
If we assume there is no power loss in the circuit, the entire input power is delivered to the load. For a constant load and input voltage, the right side of above equation is constant. Fig. 3, shows a typical $\eta - T_{on}$ profile. Any point on $\eta - T_{on}$ between $\eta_{max}$ and $T_{on,max}$ can be used to deliver power to the load. Outside of this range, we exceed maximum values of $T_{on}$ or $\eta$ and the inductor current is saturated.

Figure 3: $\eta$-$T_{on}$ profile for a fixed load

Lowering the load resistance shifts the $\eta$-$T_{on}$ profile to the right and the acceptable range becomes smaller, Fig. 4.

Figure 4: $\eta$-$T_{on}$ profile for variable loads

The maximum power that can be delivered to the load without current saturation is
1.2 Procedure

Step 1 – Find restrictions
  Measure actual inductance of inductor
  • Build the circuit according to Fig. 5 (use 50 Ω rheostat as load )
    Calculate maximum duty cycle for $V_{in}=25 V_{dc}$ and $V_o=5\pm0.5 V$
  • Measure inductor saturation current
    o Monitor inductor current using voltage drop across 1Ω resistor
    o Apply a 10 KHz, 0-5 V square wave to the gate of MOSFET switch
    o Adjust duty cycle to reach saturation level ($I_{sat}$)
    o Make sure inductor current drops to zero during the switch OFF period
    o Calculate the maximum ON time
  • Calculate maximum deliverable power and corresponding load current and load resistance

Step 2 – Constant frequency control
  • Calculate the switching frequency that delivers maximum power
  • Start with 50 Ω load, calculate the corresponding duty cycle
  • Test the circuit, do fine tuning if needed
  • Collect a few data points by increasing the load up to the maximum point, adjust $\eta$ to maintain correct output voltage

Step 3 – Constant ON time control
  • Use the ON time for maximum power
  • Start with 50 Ω load, calculate corresponding frequency and duty cycle
  • Test the circuit, do fine tuning if needed
  • Increase the load (lower the resistance), recalculate new switching parameters
  • Repeat the test to collect a few data points

![Figure 5: Flyback circuit for measurements](image-url)
<table>
<thead>
<tr>
<th>Equations</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{in} = \frac{V_{in} \cdot I_{peak} \cdot \eta}{2}$</td>
<td>Total power delivered from input DC power source during the switch ON periods</td>
</tr>
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<td>$P_{ind} = \frac{V_{o} \cdot I_{peak} \cdot (1 - \eta)}{2}$</td>
<td>Total power delivered by inductor during the switch OFF periods</td>
</tr>
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<td>$P_L = \frac{V_o^2}{R_L} = V_o \cdot I_L$</td>
<td>Total power delivered to load</td>
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</tr>
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<td>$T_{on,max} = \frac{L \cdot I_{sat}}{V_{in}}$</td>
<td>Maximum switch ON time, for a specific input voltage</td>
</tr>
<tr>
<td>$\eta_{max} = \frac{V_o}{V_o + V_{in}}$</td>
<td>Assumption: $P_{ind} = P_L$</td>
</tr>
<tr>
<td></td>
<td>Higher duty cycles leave smaller OFF time to discharge inductor current completely and cause early inductor current saturation</td>
</tr>
<tr>
<td>$f = \frac{V_{in}^2 \cdot \eta^2}{2 \cdot L \cdot P_L}$</td>
<td></td>
</tr>
<tr>
<td>$\eta = \frac{2 \cdot L \cdot P_L}{V_{in}^2 \cdot T_{on}} = \sqrt{\frac{2 \cdot L \cdot P_L \cdot f}{V_{in}}}$</td>
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</tr>
<tr>
<td>$V_{rip} = \frac{V_o \cdot \eta}{f \cdot R_L \cdot C}$</td>
<td></td>
</tr>
</tbody>
</table>
2 Isolation

A problem with the flyback circuit in Fig. 5 is that there is no isolation between the input voltage and the output voltage; failure of the diode could lead to a direct connection between input and output. If the input is derived directly from a.c. line voltages, there is a potential safety hazard. Replacing the inductor with a transformer is one way to achieve isolation as shown in Fig. 6. Another advantage of the isolation is that one side of the output can now be grounded.

![Flyback circuit incorporating a transformer](image)

The transformer must be of a special type that can work efficiently at higher frequencies (hundreds of KHz) and still transfer a respectable amount of power.

The operation of this circuit is basically the same as the previous version. During the period when the switch is closed, current ramps up in the primary storing energy in the magnetic field. The linear increase in current causes a constant voltage to appear across the secondary, but this voltage reverse biases the diode (note the dots on the transformer), and the load current is supplied by the capacitor. When the switch opens the current falls in the primary inducing a voltage in the secondary that forward biases the diode. Current flows into the capacitor transferring the energy from the transformer to the capacitor.

A simple power flow analysis of the circuit leads to the same equation for $V_{out}$ (Is the inductance that of the primary or the secondary?). However, the transformer turns ratio between primary and secondary means that the voltages on the input side will differ from those of the output side.

2.1 Transformer Configuration

For proper operation of SMPS with a transformer, similar to pervious section:

- During switch ON time, primary current must stay below saturation level:

  $$T_{on,max} = \frac{L_p \cdot I_{sat}}{V_{in}}$$

- During switch OFF time, secondary current must drop to 0:

  $$\eta_{max} = \frac{V_o}{V_o + n \cdot V_{in}}$$

where $n$ is the transformer turns ratio, $n = \frac{N_s}{N_p} = \sqrt{\frac{L_s}{L_p}}$.
For switching parameters for any load less than the maximum load

\[ \eta \cdot T_{on} \leq \eta_{max} \cdot T_{on,max} \]

\[ \frac{2 \cdot L_p \cdot P_L}{V_{in}^2} \leq \frac{V_o}{V_o + n \cdot V_{in}} \cdot \frac{L_p \cdot I_{sat}}{V_{in}} \]

Rearranging the above equations gives

\[ n \leq \left( \frac{V_o}{V_{in}} \right) \cdot \left( \frac{V_{in} \cdot I_{sat}}{2 \cdot P_L} - 1 \right) \]

\( P_L \): Maximum load power (design target)

2.2 Procedure

Transformer configuration
- Input DC voltage: \( V_{in} = 20V \pm 1 \)
- Output voltage: \( V_o = 5V \pm 5\% \)
- Output Power: \( P_L = 1W \)
- Measure actual inductance of all windings
- Monitor saturation current
  - Build a circuit according to Fig. 6
  - Use 50Ω load
  - Use 1-3, 2-3, 4-5 as primaries and 12-13 for secondary
  - **Explain your observation**
- Find at least 3 transformer configuration with a proper turns ratio

Circuit test
- Select one configuration and modify your circuit
- Start with 50 Ω load, use constant frequency control to maintain output voltage up to maximum load power.
- **Demonstrate working system to lab instructor**
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</tr>
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<td>$P_{in} = \frac{V_{in} \cdot I_{peak} \cdot \eta}{2}$</td>
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<tr>
<td>$\eta = \frac{2 \cdot L_p \cdot P_L}{V_{in}^2 \cdot T_{on}} = \frac{\sqrt{2 \cdot L_p \cdot P_L \cdot f}}{V_{in}}$</td>
<td>Assumption: $P_{in} = P_L$</td>
</tr>
<tr>
<td>$\eta_{min} = \frac{2 \cdot L_p \cdot P_L}{V_{in}^2 \cdot T_{on,max}}$</td>
<td>For a specific load, lower duty cycles cause inductor current saturated</td>
</tr>
<tr>
<td>$\eta_{max} = \frac{V_o}{V_o + n \cdot V_{in}}$</td>
<td>Assumption: $P_{ind} = P_L$</td>
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Snubber Circuits

Parasitic elements of practical component often cause undesirable effects in electronic/electrical systems. In switching mode power supplies it appears as oscillation that can cause damage to MOSFET switches. Snubber circuits are designed to reduce effects of circuit oscillation.

This section is based on application notes AN-4147 and AN-11160. It provides two different approaches to design snubber circuits. For more detail discussion refer to original documents.

**SMPS with Practical Elements**

*Figure 1* shows a Fly-back converter with some of parasitic elements that have major role in circuit oscillation.

---

\[
f = \frac{V_{in}^2 \cdot \eta^2}{2 L_p \cdot P_I}
\]

---

**Figure 1: Flyback converter with parasitic components**

- \(L_{1k}\): leakage inductor of primary
- \(L_m\): magnetized inductor of primary
- \(C_{oss}\): MOSFET output capacitance
- \(\alpha\): transformer ratio \(\left(\frac{N_p}{N_s}\right)\)

What are typical values for \(C_{oss}\), \(L_m\) and \(L_{1k}\) of the components in your design?
Oscillation

When the MOSFET switch is ON, voltage across $C_{oss}$ is very low. When it turns off, primary current quickly charges $C_{oss}$ and increases drain-source voltage. When $V_{ds}$ reaches to $V_{in} + a.V_{o}$, voltage across $L_m$, is $a.V_{o}$ and secondary voltage is $V_{o}$. Secondary diode, $D_1$, starts conducting. Output capacitor clamps primary and secondary voltages at fixed levels, Figure 2.

![Figure 2: Voltage levels when secondary diode starts conducting](image)

Forcing voltage across $L_m$ to a DC level, resembles applying Step input to the LC oscillator composed of $L_{lk}$ and $C_{oss}$, that causes oscillation. The oscillation frequency is:

$$f_{lk} = \frac{1}{2\pi\sqrt{L_{lk} \cdot C_{oss}}}$$

The voltage on drain is:

$$V_{ds} = V_{in} + n.V_{o} + V_{osc}$$

The oscillation causes high voltage peaks and over time can cause damage to the MOSFET, Figure 3.
Circuit Design

1.1.1 Parasitic elements
To design a snubber circuit, first we need to determine $L_{lk}$ and $C_{oss}$:

- **Step 1:** Find the resonance frequency after switch turns off ($f_1$)
- **Step 2:** Add a capacitor between drain and source
- **Step 3:** Measure the new resonance frequency ($f_2$)
- **Step 4:** Use equation below to determine $C_{oss}$ and $L_{lk}$

$$C_{oss} = \frac{C_{add}}{\left(\frac{f_1}{f_2}\right)^2 - 1}$$

$$L_{lk} = \frac{1}{(2\pi f_1)^2 C_{oss}}$$

Are $L_{lk}$ and $C_{oss}$ in the acceptable range?

1.1.2 RC Snubber Circuit
By adding a resistor and capacitor between drain and source, we creates a RLC circuit that can damp the oscillation, *Figure 4.*
The step response of a RLC circuit is depicted in Figure 5.

Figure 5: Step response of RLC circuit

For overdamped operation, $\zeta$ must be greater than 1. High damping factors make circuit more sluggish. So there is practical limit on how large $\zeta$ can be. Damping factor and cutoff frequency for the RLC is approximated using following equations:

$$\zeta = \frac{1}{2R_s \sqrt{\frac{L_{ik}}{C_{oss}}}}$$
\[ f_c = \frac{1}{2\pi R_s C_s} \]

Note: both equations are simplified forms. \( C_s \) and \( C_{oss} \) are not considered in equations for Damping Factor and cutoff frequency.

- **Circuit Design**
  - **Step 1**: Select an initial value for \( \zeta \), calculate \( R_s \)
  - **Step 2**: Select a cutoff frequency, calculate \( C_s \)
  - **Step 3**: Test your circuit and change \( \zeta \) and/or \( f_c \) if required

### 1.1.3 RCD snubber Circuit

RCD snubber circuit protects MOSFET switch from overvoltage damage by limiting maximum voltage drop across the switch. Figure 6 shows RCD snubber circuit added to primary side of the transformer. When drain voltage raises to \( V_{in} + V_{sn} \), \( D_{sn} \) conducts and primary current redirect to the snubber circuit. \( C_{sn} \) clamps drain voltage to \( V_{in} + V_{sn} \).

![Figure 6: Snubber circuit](image)

*Figure 6: Snubber circuit*

*Figure 7 shows drain pin voltage after implementing proper snubber circuit.*
Figure 7: voltage on drain pin is limited by snubber circuit

- **Circuit Design**
  - Calculate power consumed in snubber circuit, i.e. $R_{sn}$:
    \[
    P_{sn} = \frac{1}{2} L i_{\text{peak}}^{2} V_m \frac{V_m}{V_{sn}} - nV_o f_s
    \]
  - $i_{\text{peak}}$: Primary peak current at the end of ON time. **Consider worst case scenario**
  - $V_{sn}$: Snubber circuit maximum voltage, consider a voltage level 1.3 to 2 times of $aV_o$.
  - $f_s$: Switching frequency
    - Calculate snubber circuit resistance, $R_{sn}$:
      \[
      R_{sn} = \frac{V_m^2}{P_{sn}}
      \]
    - Calculate snubber circuit capacitance, $C_{sn}$:
      \[
      C_{sn} = \frac{V_m}{\Delta V_{sn} R_{sn} f_s}
      \]
    - Where $\Delta V_{sn}$ is the acceptable ripple voltage across $C_{sn}$ In general 5-10% ripple is reasonable
  - **Diode, $D_{sn}$**: What parameters must be considered in selecting proper diode?

**Procedure**
- Use your circuit from Section 0
- Follow instruction to find parasitic elements values.
- Select one method and design the circuit. Include calculation in your report
- Test the circuit and presents waveforms to show improvements
Design of a regulated supply

In previous parts, the circuit was not a regulated power supply since the output voltage changed with the load. A regulated supply will have additional circuitry that senses the output voltage and automatically adjusts the switching frequency or duty cycle to maintain a constant output. Semiconductor manufacturers have developed ICs that perform SMPS regulation.

Design hints

Error! Reference source not found. shows simplified block diagram of a regulated power supply (for the purpose of this lab).

- The step down transformer provides isolation for safety and reduces the AC voltage to 24V.
- The rectifier circuit rectifies the AC input, a half-wave or full-wave rectifier can be used for this stage.
- A filter capacitor is required to produce unregulated d.c. input voltage for next stage. The capacitance will determine the ripple on the unregulated voltage;
  \[ V_{rip} = \frac{I}{C \cdot f} \]
  where I is the average current draw, and f is the frequency (60 Hz for half-wave and 120 Hz for full-wave rectification).
- The integrated regulator IC available to you is from STMicroelectronics’s UC384xB family, specifically the UC3845B. You will need to read the datasheet for the regulator IC. Yes, it is not very clear (actually the datasheet from ON Semiconductor is somewhat better than the one from STMicroelectronics). But datasheets are all too often poorly written, so this exercise is good practice.

1.1.4 Controller chip

The controller regulates the voltage by adjusting the duty cycle at a fixed switching frequency which is a form of pulse width modulation (PWM). The controller computes the proper duty cycle based on two control loops; one that senses the current in the inductor (input pin 3) and one that senses the output voltage (input pin 2). Both of these feedbacks need to be wired for the chip to work. The computed PWM signal controls the switching MOSFET (output pin 6) (see Fig. 3-1).
Figure 16 of datasheet (ON Semiconductor) shows the basic circuit for using the IC and includes connections to power, ground, the MOSFET, the current sense resistor, the voltage feedback, and an RC network to set the frequency.

The current sense resistor generates a voltage proportional to the current through the inductor during the first part of the cycle (switch closed). The value of the sense resistor ($R_s$) must be selected such that $I_{\text{peak}} \times R_s < 1.0 \text{ V}$. You can protect the current sense input with a voltage limiter (1.0 V zener diode).

The voltage control compares the voltage feedback signal to a 2.5 V reference that is generated internally. The output voltage needs to be scaled to 2.5 V to provide the feedback signal. Scaling can be done using a simple voltage divider. The total resistance of the divider should be large enough to present a minimal additional load on the output.

An internal oscillator controls the switching frequency; the oscillator's frequency is set by an RC circuit connected to pins 4 and 8 (Figure 16 of the datasheet). Note that the switching frequency is half the internal oscillator's frequency. The capacitor also controls the maximum duty cycle.

OK so how do you choose $R$ and $C$? You must decide on the switching frequency and maximum duty cycle based on the output voltage and maximum current draw by the load as you did in part 1. Then choose $C$ to give the required maximum duty cycle based on the graph in Fig. 3 on page 4. Note that % output deadtime is the opposite of duty cycle, $\%DT = 1 - \eta$. Once you have $C$ then choose $R$ to give the correct oscillator frequency using the graph in Fig. 2 on page 4. If your resistor will be greater than 5K then you can instead use the formula below the graph in Fig. 2 to calculate $R$. Remember that the switching frequency is half the oscillator frequency.
Important figure and tables (Datasheet from ON Semiconductor)

- The PIN FUNCTION DESCRIPTION table on page 6 provides a brief but useful description of UC3486B pins.
- The MAXIMUM RATINGS table on page 2 must be considered during the design process (e.g. the maximum voltage that can applied to the IC).
- The Design Considerations section on page 9 provides some general design hints, especially on how to use bypass capacitors for noise reduction.
- Fig. 30 shows a better current feedback circuit where a RC filter is added to the current sense input to eliminate narrow spikes on the leading edge of the current waveform. The spikes decrease the stability of the current control loop. For more details refer to the “Current Sense Comparator and PWM Latch” section on page 7.

1.1.5 Design Constraints
Another restriction on transformer turns ratio enforced by the current controller IC. UC3845 can generate square waves with maximum 50% duty cycle, i.e.:

$$\frac{V_o}{V_o + n.V_{in}} \leq 0.5$$

Rearranging the above in-equation gives:

$$n \geq \frac{V_o}{V_{in}}$$

Thus the valid range for turns ratio is:

$$\left( \frac{V_o}{V_{in}} \right) \leq n \leq \left( \frac{V_o}{V_{in}} \right) \left( \frac{V_{in} \cdot I_{sat}}{2 \cdot P_L} - 1 \right)$$

Consider other maximum rating hat can affect your design.

Procedure
Objective: Design a 5V, 1W power supply. The output ripple must be less than 2%

- Input stage design: design rectifier module, find proper transformer configuration, and calculate input filter capacitor. How much ripple can the SMPS take at its input (tricky question)?
- Flyback circuit: Use flyback circuit with isolation in section 0, modify it to add current and voltage loops
- Controller module: calculate switching parameters, and design controller IC peripherals according to datasheet
- Design snubber circuit
- Test each module independently whenever it is possible
- Integrate all modules and test the complete circuit. Start with 50 Ω load, and increase the load up to 1W
- Demonstrate working system to lab instructor.