Euler Path for Optimal Layout

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Outline:
- Optimized approach
- Graph-theoretical algorithm
- Heuristics
- Conclusion
- References

Optimized approach (Euler Path)
- The Euler path technique has been used in what is called the “standard cell technique”, which results in a dense layout for CMOS gates and one polysilicon strip that can serve as the input to both NMOS and PMOS devices.
- Our main aim is to have a single strip of diffusion in both NMOS and PMOS devices. This depends on the “ordering” of the inputs. How do we determine the best order?

Two Versions of $\overline{C} \cdot (A + B)^1$
(Observe the input order)
Graph the theoretical approach

- To reduce the size of an array and an uninterrupted diffusion strip we need to find this “Euler path” talked about previously. This is defined as the path through all nodes or vertices (source and drain signals) such that each edge (transistor gate inputs) is only visited exactly once. (vertices maybe visited more than once).
- Euler paths are not unique.
- Euler paths must be consistent (same ordering in both PUN (pull up network) and PDN (pull down network)).
- Can Run in linear time

Consistent Euler Path

The General Algorithm

1. Enumerate all possible decompositions to find the minimum number of Euler paths that cover the graph.
2. Chain by means of diffusion area according to the order of edges in Euler path.
3. If more than 2 edges are necessary to cover the graph model, then provide a separation area between each pair of chains.

Heuristic Algorithm

(of course life not being so easy)

Theorem:

1) The following example and any circuit will have a single Euler path if the number of inputs to every AND/OR element is odd. In addition,
2) There exist a graph model such that the sequence of edges on an Euler path corresponding the vertical order of the inputs on a planar representation of the logic diagram.
3) Construct the graph model according to the vertical order of inputs on logic diagram.
4) Chain together the gates by means of diffusion areas as indicated by the sequence of edges on the Euler path. A “pseudo” input gives a separation between diffusions.
5) Delete “Pseudo” edges in parallel and contacting “pseudo” edges in series with other edges for final circuit.
Example

We consider the following logic Circuit (a and b), the derived Euler Path (c) and the corresponding Layout. For our Euler path the PIN and the PDN.

Heuristic Works

We apply our Heuristic approach to the previous example and we obtain the following sequence (p1,2,3,4,5,p2) where we remove the “pseudo” inputs to get the same layout previously shown in slide 11. (Note we choose the combination with the minimum interlaced with real inputs) hence circuit (b).

Analysis

1. It must be noted that the heuristic algorithm may not always give the optimal layout but if the resulting sequence. However, if no separation areas are obtained then this is the optimal solution.

2. The heuristic gives excellent results for circuits which do not have a Euler path. This is illustrated in the four-bit carry look-ahead adder circuit shown in this slide.

Analysis (continued)

Here in (b) we see the final Euler Path interpretation the corresponding circuit diagram (c) and the a final layout.
Conclusion

- This Presentation has given a brief incite into optimizing the layout of complex CMOS gates. Using the Euler path approach and a heuristic algorithm. The results show that by use of this approach we can optimize considerably on area in our layout. Further work can be done to simulate the “real” gain of this method in terms of power and performance of a particular design.

References

1. Digital integrated circuits 2nd edition
2. Uehara, T. and Vancleemput, W. M “optimal layout of CMOS Functional Arrays”.